1. **Define Moore’s Law**

**Moore's law** is the observation that [the number](https://en.wikipedia.org/wiki/Transistor_count) of [transistors](https://en.wikipedia.org/wiki/Transistor) in a dense [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit) (IC) doubles about every two years. Moore's law is an [observation](https://en.wikipedia.org/wiki/Observation) and [projection](https://en.wikipedia.org/wiki/Forecasting) of a historical trend. Rather than a [law of physics](https://en.wikipedia.org/wiki/Physical_law), it is an [empirical relationship](https://en.wikipedia.org/wiki/Empirical_relationship) linked to [gains from experience](https://en.wikipedia.org/wiki/Wright%27s_Law) in production.

The observation is named after [Gordon Moore](https://en.wikipedia.org/wiki/Gordon_Moore), the co-founder of [Fairchild Semiconductor](https://en.wikipedia.org/wiki/Fairchild_Semiconductor) and CEO and co-founder of [Intel](https://en.wikipedia.org/wiki/Intel), who in 1965 posited a [doubling every year](https://en.wikipedia.org/wiki/Exponential_growth) in the number of components per integrated circuit,[[a]](https://en.wikipedia.org/wiki/Moore%27s_law#cite_note-2) and projected this rate of growth would continue for at least another decade. In 1975, looking forward to the next decade, he revised the forecast to doubling every two years, a [compound annual growth rate](https://en.wikipedia.org/wiki/Compound_annual_growth_rate) (CAGR) of 40%. While Moore did not use empirical evidence in forecasting that the historical trend would continue, his prediction held since 1975 and has since become known as a "law."

1. **Physical Limitations**

**Dennard scaling ignores the leakage current and threshold voltage.**

**Moore's Law** was originally developed purely for describing the number of transistors that could be put on a chip at minimal cost. The problem for chip designers is that Moore's Law depends on transistors shrinking, and eventually, the laws of physics intervene. In particular, electron tunnelling prevents the length of a gate - the part of a transistor that turns the flow of electrons on or off - from being smaller than 5 nm. The other problem hindering smaller transistors is heat extraction. The more transistors there are on a chip, the more heat it produces, and the greater the chance of a malfunction. New methods must be developed to remove that heat from the chip.

Intel researchers published a paper in 2003 called [Limits to Binary Logic Switch Scaling - a Gedanken Model](http://download.intel.com/technology/silicon/Bourianoff-Proc-IEEE-Limits.pdf). The paper anticipated that the industry would reach the limits of Moores law, and said that a trade-off between density and speed would be necessary to keep extending it.

**Voltage Scaling cannot prevent leakage power loss.**

**Hard drive storage** has suffered from similar problems to electronic transistors on chips. The devices store information magnetically using a series of ones and zeros. They use grains of magnetic material to store this information. Storage vendors have continued to increase the density of the magnetic grains on a hard drive by making them smaller. However, as density approaches 100 Gb per square inch, the physical law of superparamagnetism looms. When small enough, the magnetic grains will alter their magnetic state unpredictably, switching ones to zeros and vice versa.

**Voltage Scaling cannot prevent leakage power loss.**

**From horizontal to vertical**

The use of carbon nano tubes and silicon-germanium nanowires could extend the performance of transistors to some extent, although their size would remain roughly the same. Another potential solution is the use of 3D chips, in which layers of transistors are stacked on top of each other. This would maintain the horizontal size of the chip, while drastically increasing its transistor count. In 2008, researchers at the University of Rochester managed to create [three-dimensional circuitry](http://www.tomshardware.com/news/rochester-3d-processor,6369.html) running at 1.4 GHz. That chip optimized the way that components interact with each other vertically, rather than simply layering banks of regular transistors on top of each other without having the different layers communicate.  
**Temparature increases as power increased**

1. Top of Form
2. Bottom of Form

On the storage side, companies such as [IBM](http://www.physorg.com/news107703707.html) and [HP](http://www.hpl.hp.com/news/2005/jan-mar/crossbar.html?jumpid=reg_R1002_USEN) have been working on both storage and computing systems that work at a molecular level. Layers of molecular strands, laid out in a grid, could also form the basis for a microprocessor.

**Voltage scaling reduces the power consumption.**

**While we wait: virtualization**

Until significant technological advances in storage appear, the innovations must come in software. Virtualization technology enables us to use more of each processors' capacity, by separating the software processes running on them into separate virtual machines, ensuring that they do not interfere with each other. This can increase processor utilization from 10-15% up to 80-90%.

Virtualization can also help us to maximise our storage capacity.

**Voltage Scaling is limited due to noise or threshold voltage**

In traditional dedicated storage environments, where one physical disk drive is allocated to a particular application, much storage capacity goes unused. Instead, we can virtualise our storage into storage area networks, in which any disk in a high-speed network can store some information for a software application. This allows us to spread our data more evenly over a lot of disk drives, minimising the unused space.